

SL1620 DDR4 Core Module RDK

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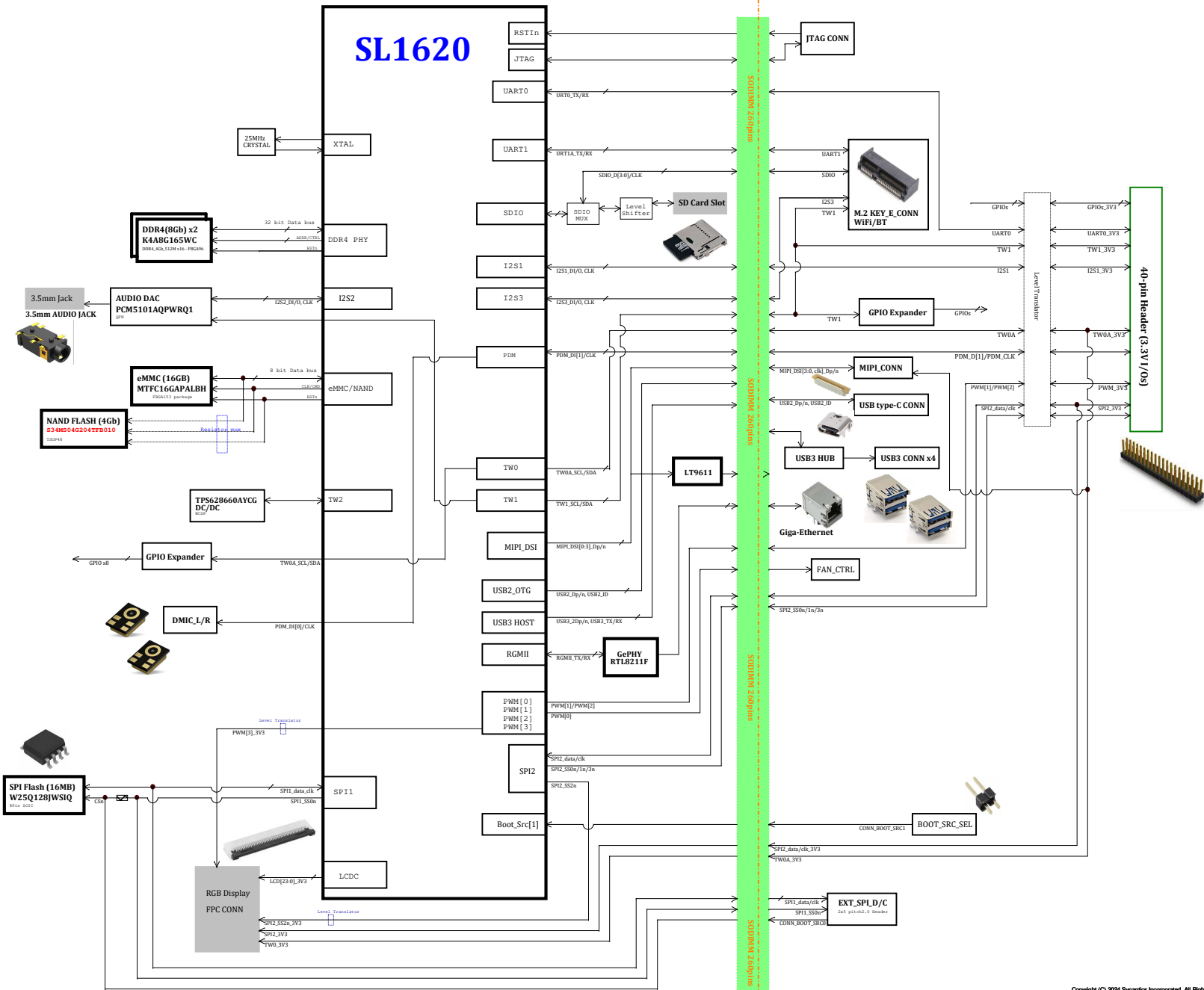
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REVISION HISTORY

Rev#	Date	Originator(s)	Rev Item ID	What Revised	Why Revised	SW Impacts	Other Impacts	Rework# Base On Previous Version	SW Strap [3:1]=b'
A	01/13/2024	Iris Fan	1	Initial Release.		NO	NO	NO	000
B	01/25/2024	Iris Fan	1	[Page.7] Adding PD resistors R1995~R2000 to unused I/Os of U83.	TMUX1574 Datasheet requirement				
			2	[Page.16] Supply 1.8V power to U92 pin#18 (LDO0).	Design issue fixed	NO	NO	Rework A	000
			3	[Page.16] Change R301 to Pull down U92 pin#12 (SCK) to enable internall PLL.	Design issue fixed				
	03/06/2024	Sheelan Zhu	1	[Page.7] 1. R41 changed to 33 ohm	EMI improvement	YES	NO	NO	000
			2	2. add R55/R59 33 ohm, C35/C81 22pF for sdio sd/m2 clk	EMI improvement				
			3	[Page.8] 1. Del RGMII CLK OUT. NC	EMI improvement				
			4	2. R65,R68, R74~R77 33 ohm on RGMII TX	EMI improvement				
			5	[Page.9] 1. R78/R79 33 ohm on I2S1 MCLK/BCLK	EMI improvement				
			6	2. R84 33 ohm on LCD CLK	EMI improvement				
			7	[Page.13] R195 changed to 33 ohm	IO Control for LT9611				
C	04/29/2024	Xiaomin Luo	1	[Page.15] 1. R211,R212,R214,R231,R232,R234 changed to 33 ohm	EMI improvement				
			2	2. 25MHz crystal for rt18211	New requirement				
			3	[Page.16] add DSI to HDMI converter	EMI improvement	Yes	NO	NO	000
			4	[Page.19] R21 changed to 33 ohm	EMI improvement				
D	06/21/2024	Xiaomin Luo	1	[Page.7/8/9/19] 1. C128,C129,C132,C133 10pF DNS by default	EMI improvement				
			2	2. C90 Stuffed by default	New requirement				
			3	[Page.22] add INA3221/INA220 to measure VCORE/VDDM_1V2/SOC_1V8/SOC_3V3 Power					
			4	[Page.18] Replace U81 to U93 directionless levelshifter TXB0104RGYR.	Design improvement	Yes	NO	NO	000
			5	Change PWM[2] and GPIO[2] to 3.3V for 40 pin Header.	Design update				
E	09/18/2024	Xiaomin Luo	1	Remove USB-C_INTn signal.	Remove useless signal				
			2	[Page.11] Stuff R119. SW_STRP[3:1] = 3'b100 for Current sensor supporting.	Update SW Strap to 3b'100				
			3	[Page.14] Fix IOEXP ADDR/RST1 connection error.	Issue fix				
			4	[Page.19] Add 0.1uF cap between Q29 D/G.	Optimize SD power sequence	Yes	NO	Rework B and C	100
			5	Add 1Kohm.					
			6	[Page.22] Remove U4.	Remove 1V8 and 3V3 here, they are measured in IO board.				
			7	Measure VCORE, 1.2V, 2.5V measurement to U9.					
			8	[Page.21] Add 4 standoffs for mounting heatsink	Manufactuer requirement				
			9						
			10						

Core Module

I/O Board

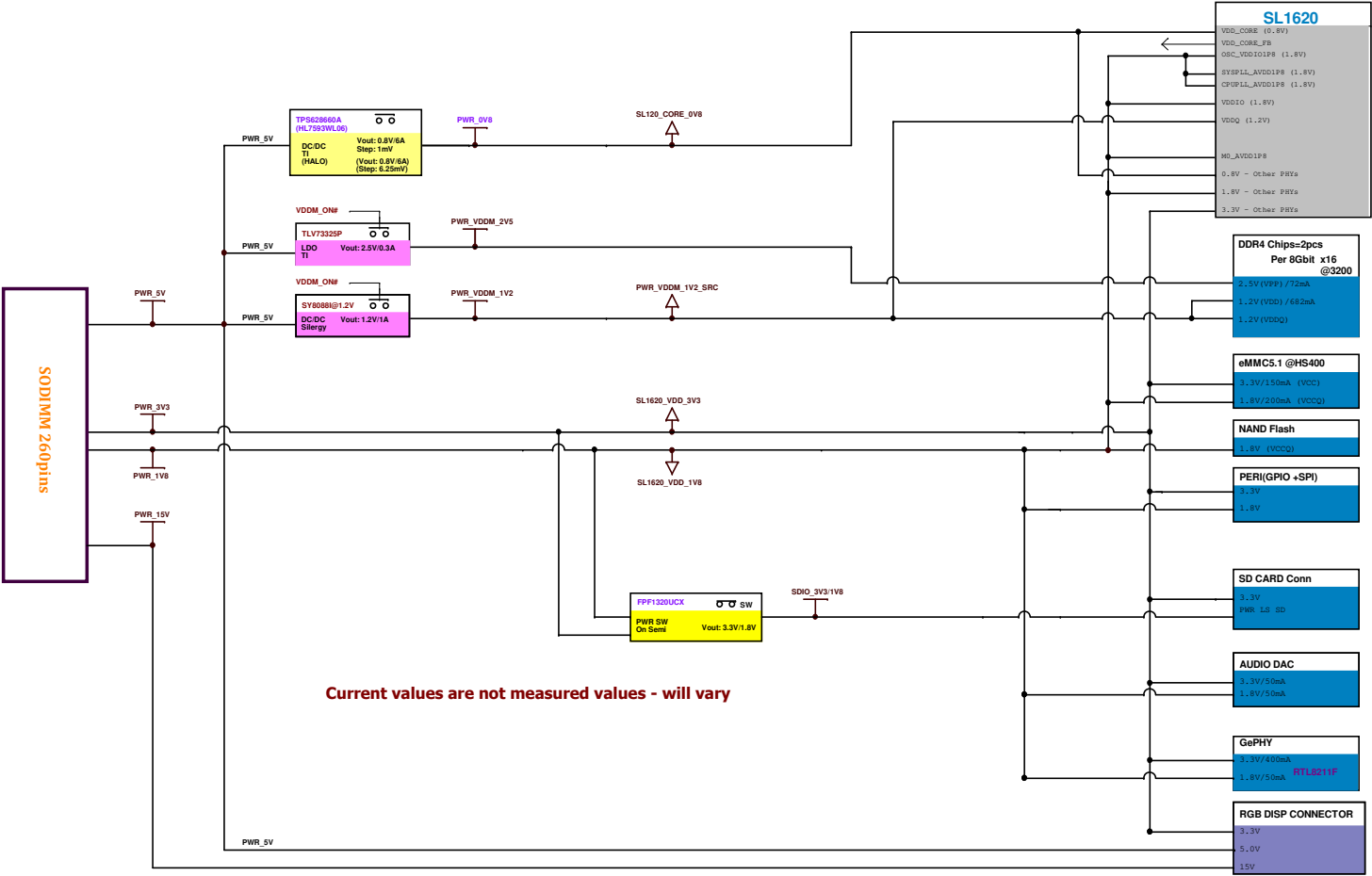


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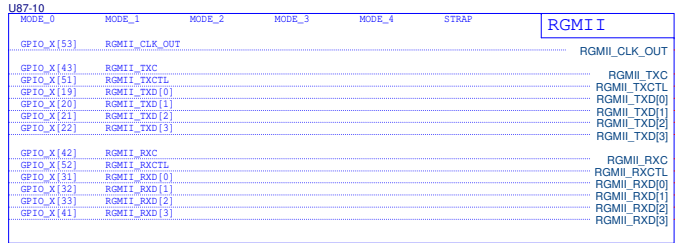
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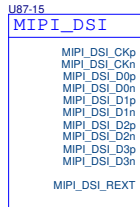
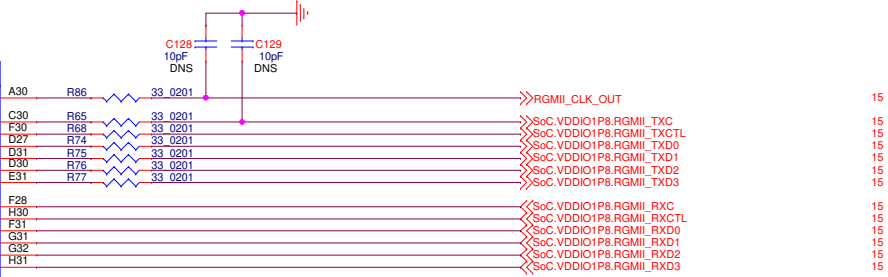
Power Tree



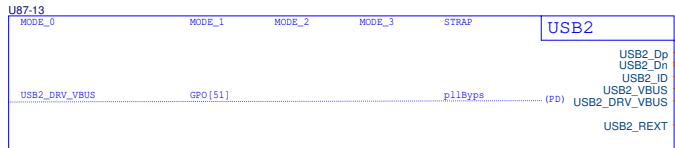




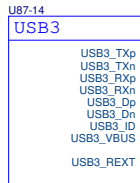
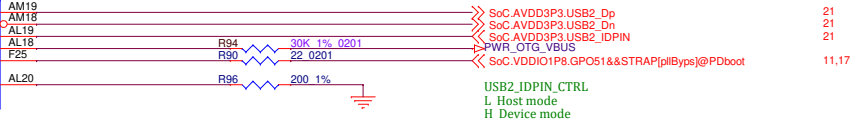
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SL1620_DDR4



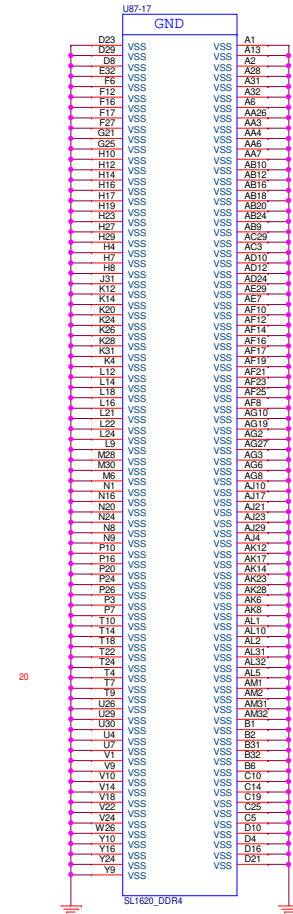
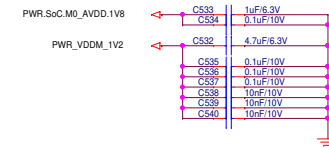
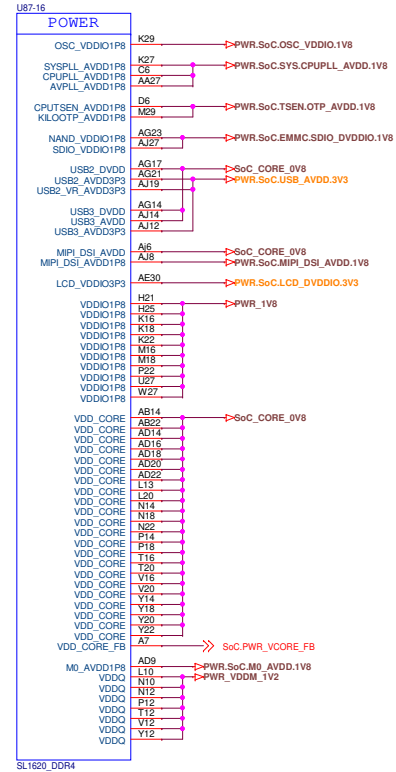
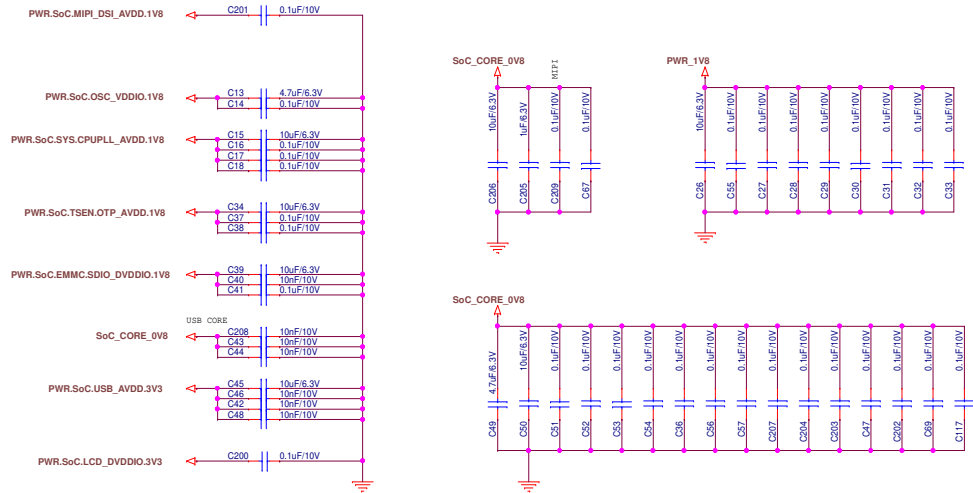
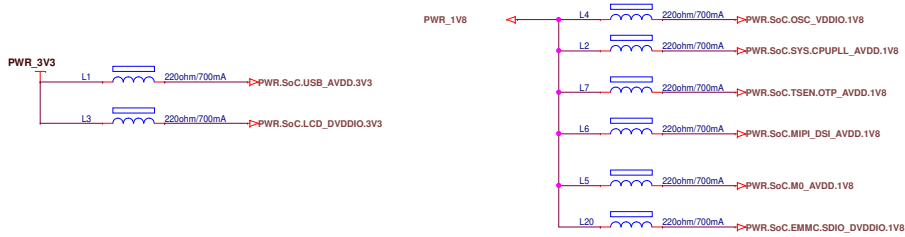
SL1620_DDR4



SL1620_DDR4



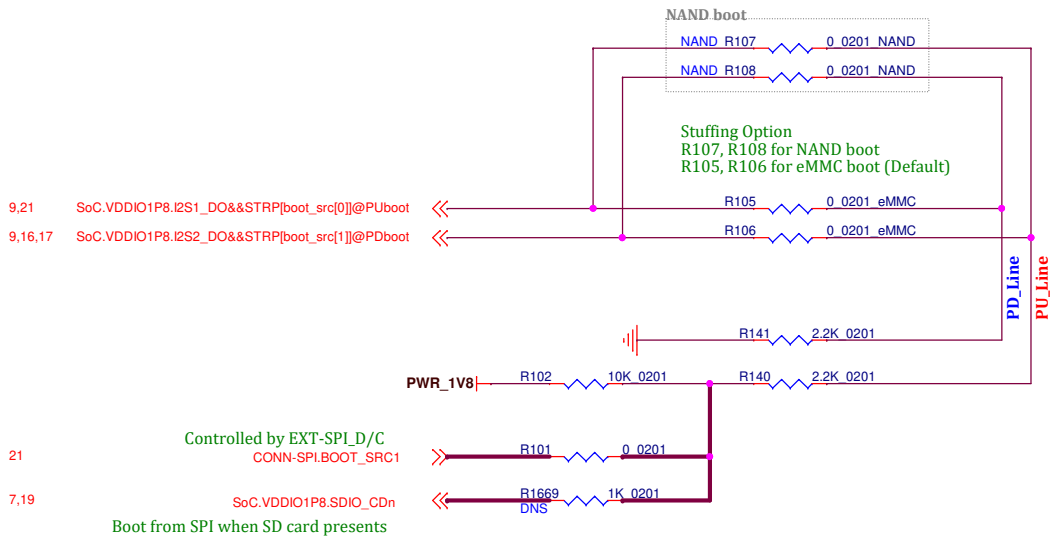
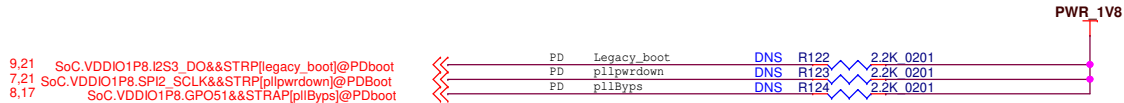
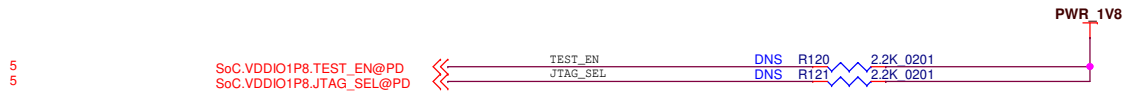
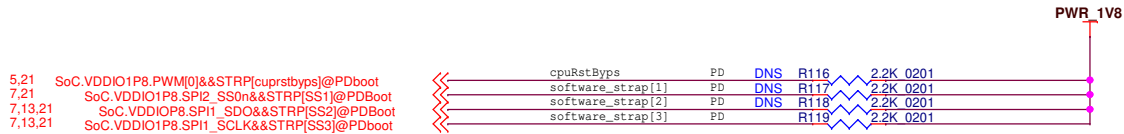
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TEST_EN 0: In function mode or JTAG mode, no SCAN mode. (Default)
1: In test mode, particular in SCAN mode.

JTAG_SEL 0: Select ICE debug mode (Default)
1: Select BSCAN TAP mode

POR_EN 0: External POR
1: Internal POR (Default)

legacy_boot 0: 2ms (Default)
1: 20ms

SW_STRAP[0] 0: Boot from USB
1: Boot from the device selected by Boot_SRC (Default)

software_strap[1]
Default: 0

software_strap[2]
Default: 0

software_strap[3]
Default: 0

cpuRstByps 0: Enable reset logic inside cpu partition (Default)
1: Bypass reset logic inside cpu partition

pilPwrDown 0: Power up SYS/MEM/CPU PLL (Default)
1: Power down SYS/MEM/CPU PLL

pilByps 0: No Bypass (Default)
1: All PLL bypassed

BOOT STRAP OPTION

BootSrc[1:0]	TYPE
2'b00	SPI-Secure Boot
2'b01	ROM boot from NAND default
2'b10	ROM boot from EMMC
2'b11	SPI-Clear Boot
SPI2_SDO = 0 USB boot	

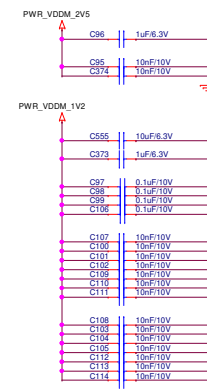
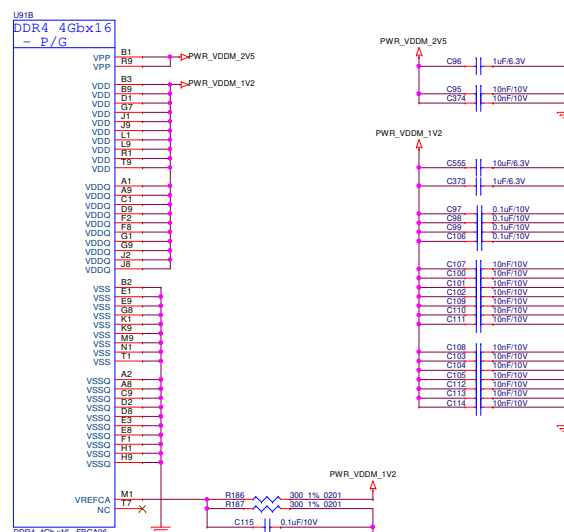
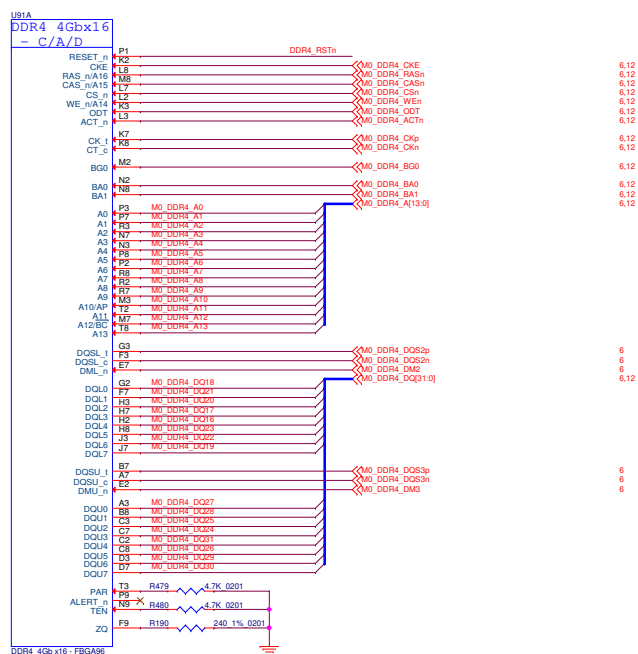
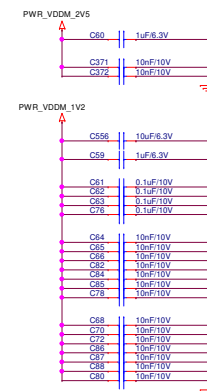
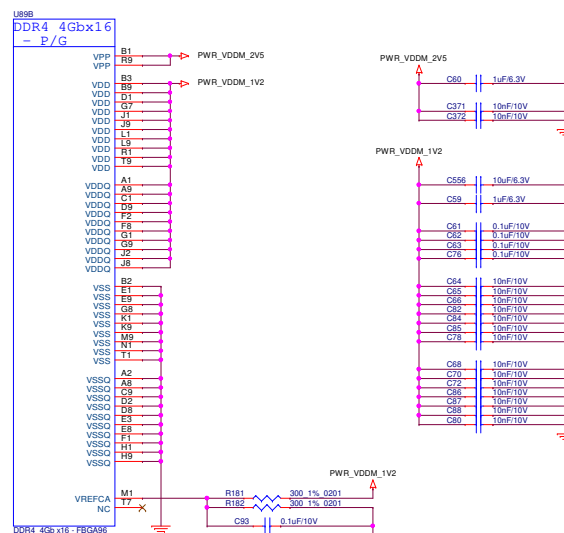
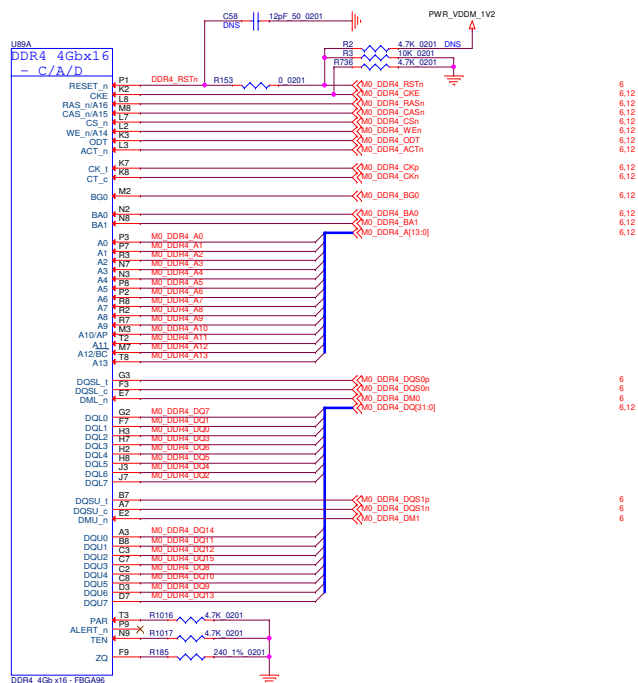
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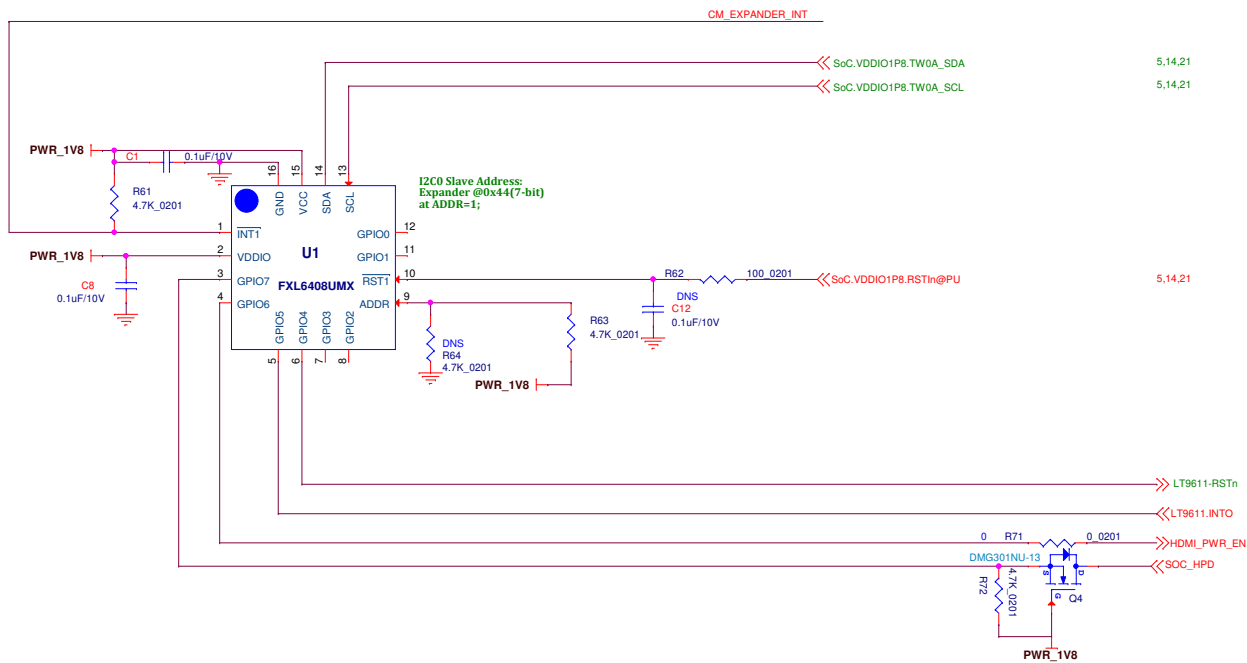
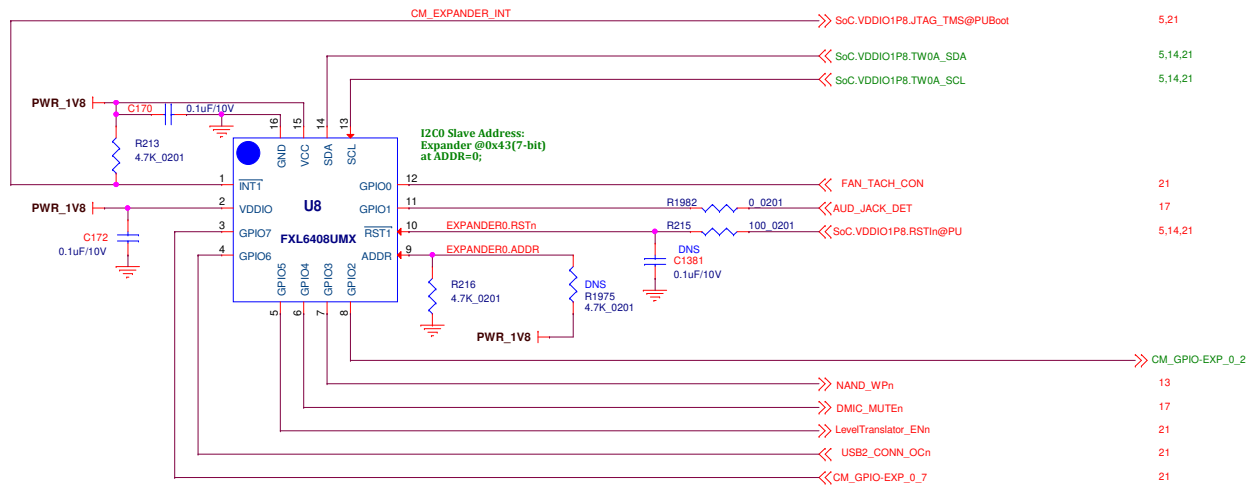
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PHY Address	PHYAD[2:0]
0x0	3'b000
0x1	3'b001
0x2	3'b010
0x3	3'b011
0x4	3'b100
0x5	3'b101
0x6	3'b110
0x7	3'b111

Hi-Z or Low
GPIO_EXP3V3.GPIO0_5_INV

PWR_1V8_RGMII-STRP
DNS R130 2.2K 0201
R133 2.2K 0201

SoC.VDDIO1P8.RGMIIA_MDC
SoC.VDDIO1P8.RGMIIA_MDIO
SoC.VDDIO1P8.RGMII_TXC
SoC.VDDIO1P8.RGMII_TXCTL
SoC.VDDIO1P8.RGMII_TXD3
SoC.VDDIO1P8.RGMII_TXD2
SoC.VDDIO1P8.RGMII_TXD1
SoC.VDDIO1P8.RGMII_TXD0

SoC.VDDIO1P8.RGMII_RXCTL

SoC.VDDIO1P8.RGMII_RXC

SoC.VDDIO1P8.RGMII_RXD3

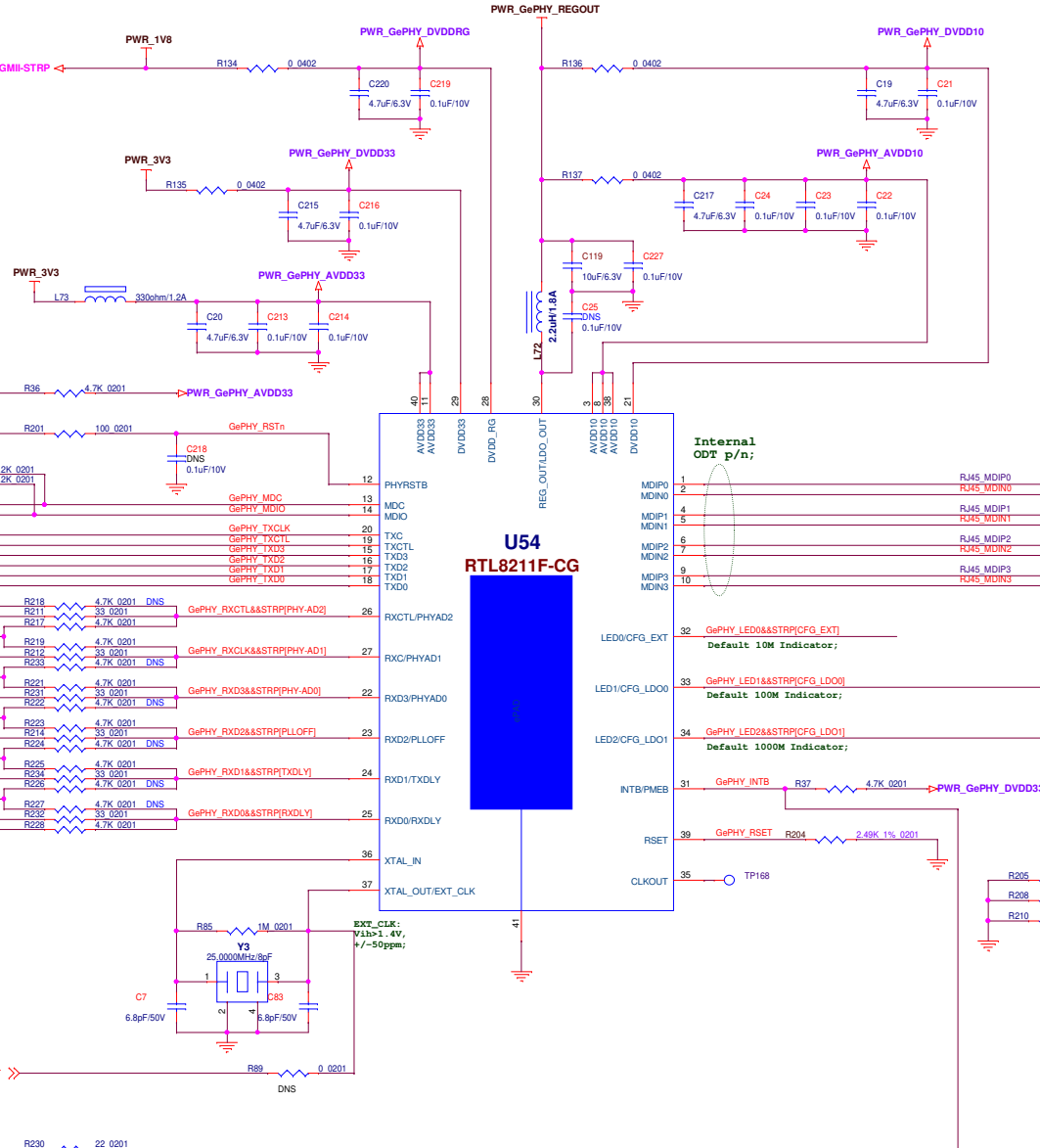
SoC.VDDIO1P8.RGMII_RXD2

SoC.VDDIO1P8.RGMII_RXD1

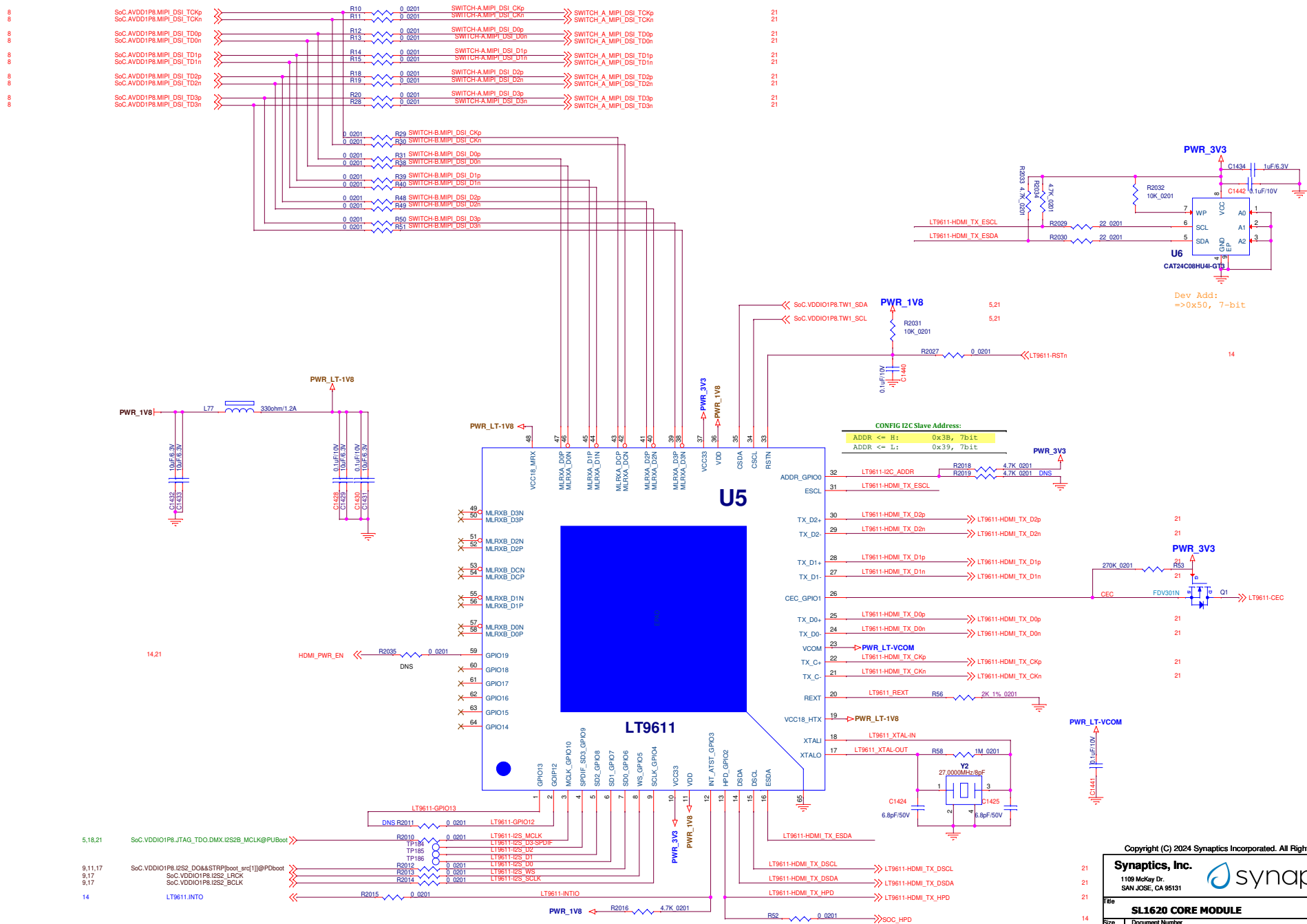
SoC.VDDIO1P8.RGMII_RXD0

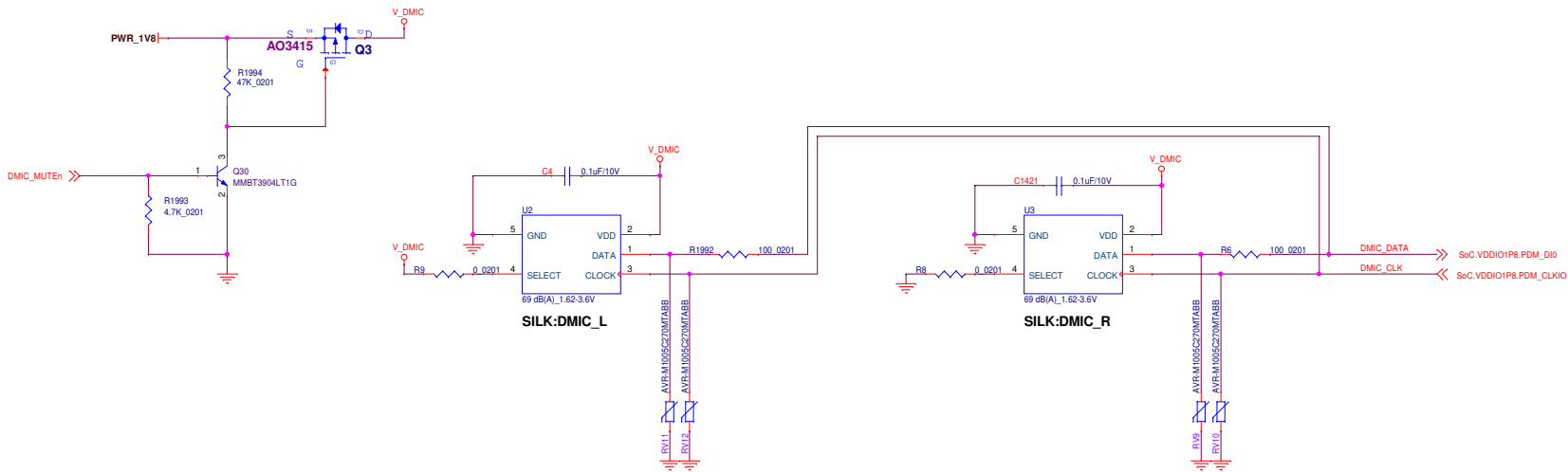
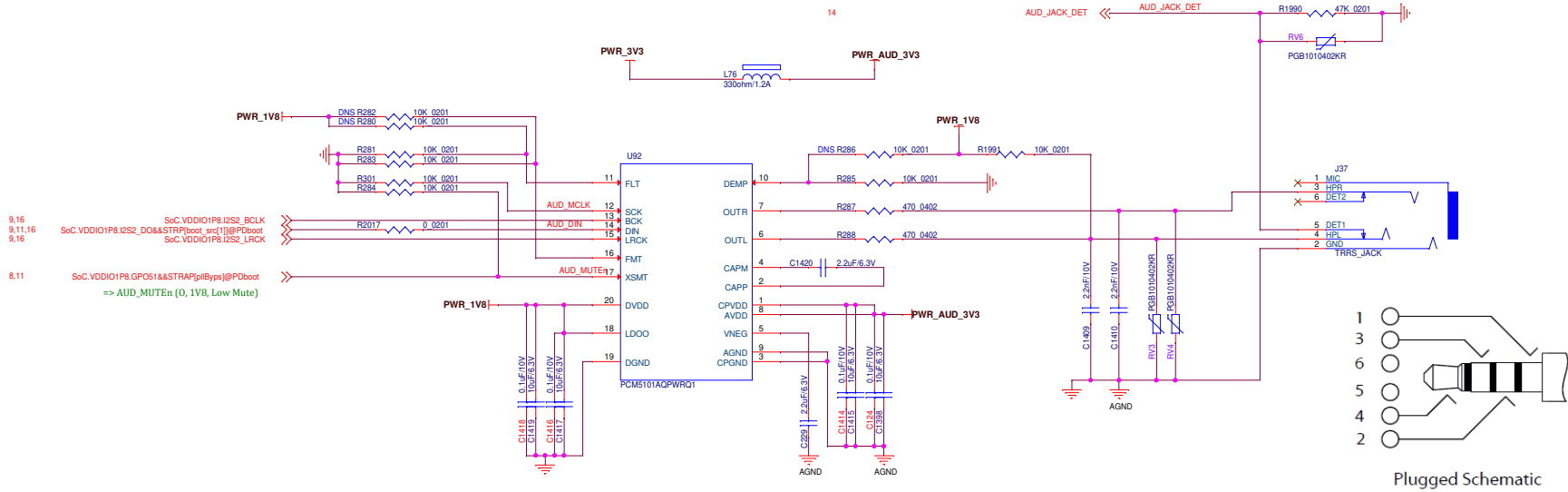
RGMII_CLK_OUT

SoC.VDDIO3P3.GPIO_X11



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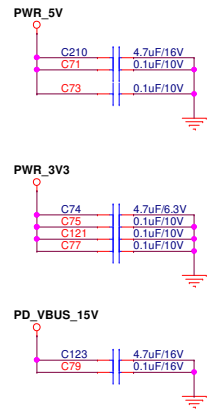




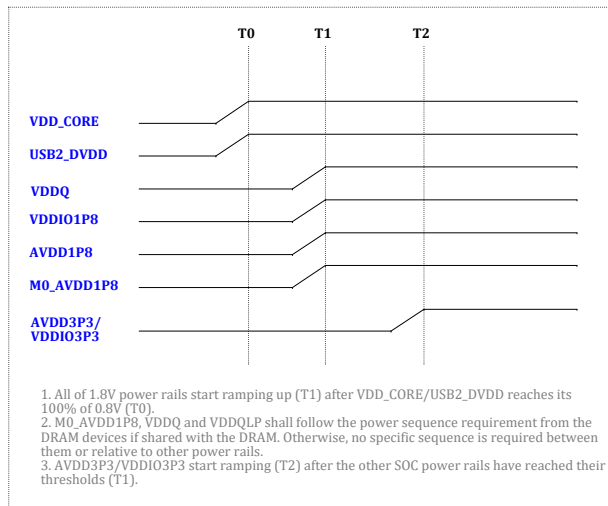
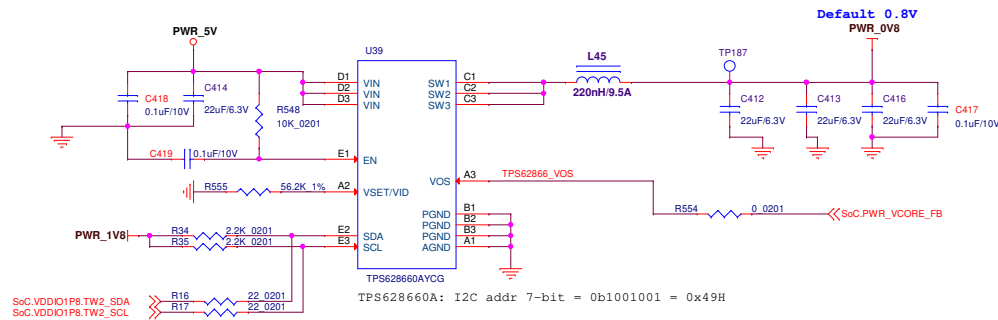
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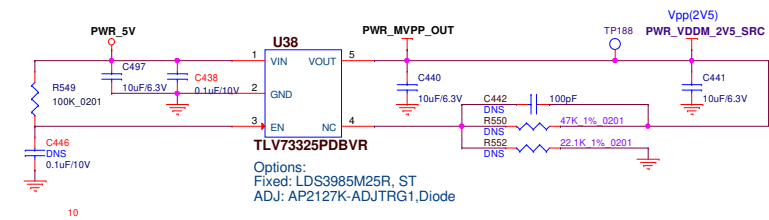


VDD_CORE POWER - 6A/5mV Step (Default)

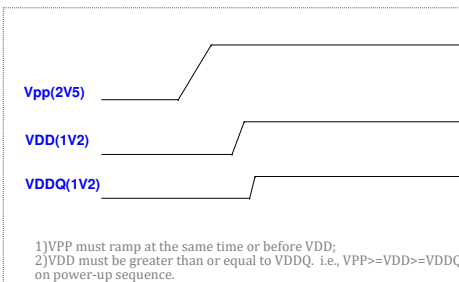
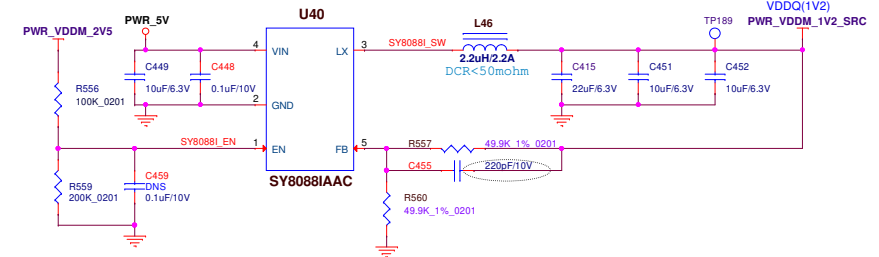


SL1620 Recommended Power Sequence

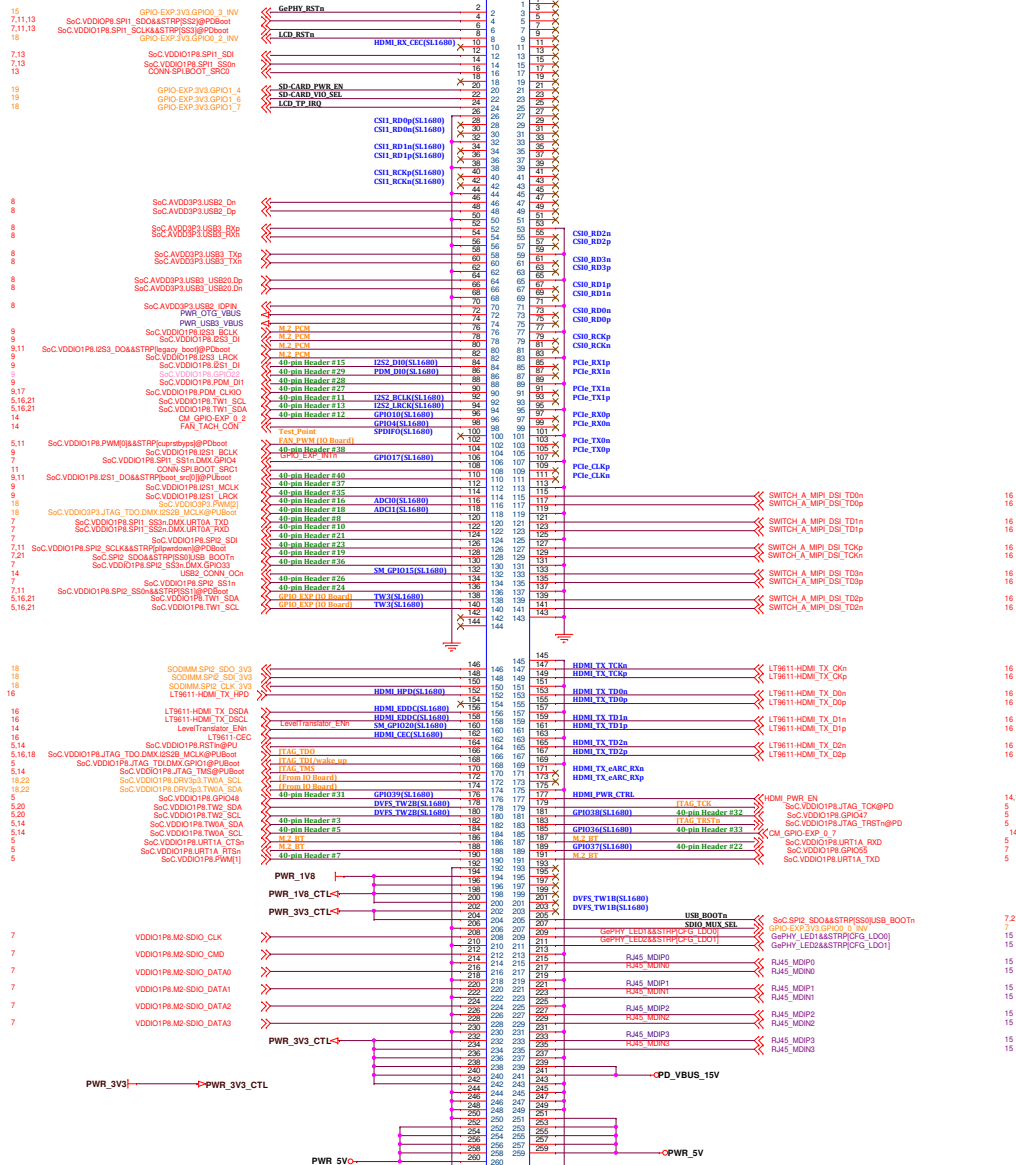
2.5V/0.3A for DDR-DEVICES;



1.2V/1A for DDR-SOC + DDR-DEVICES;

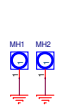
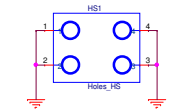
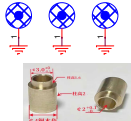


Power-Up Sequence For DDR4 DEVICE



Overlap with Holes_HS

STO1 STO2 STO3 STO4
StandOff StandOff StandOff StandOff

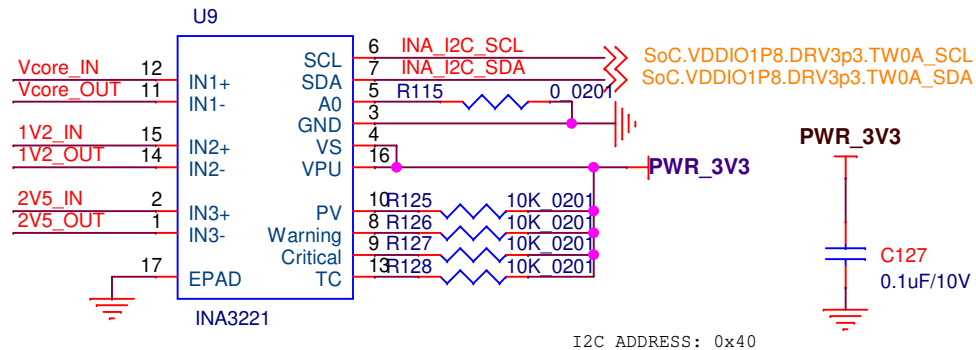
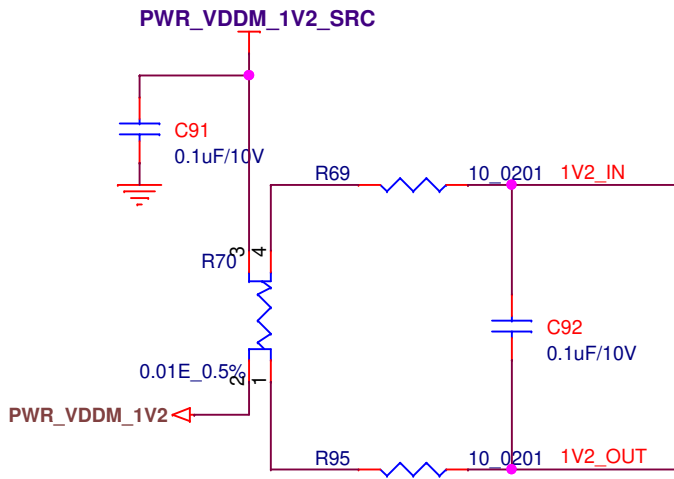
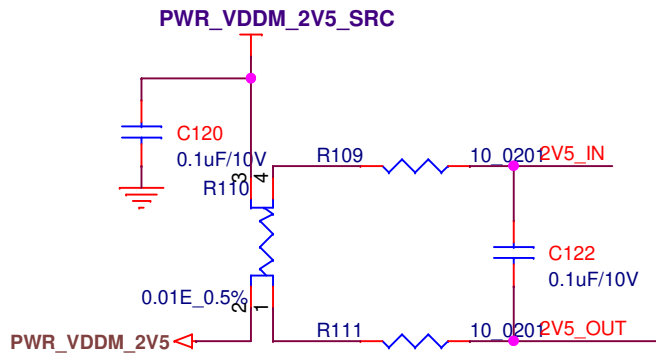
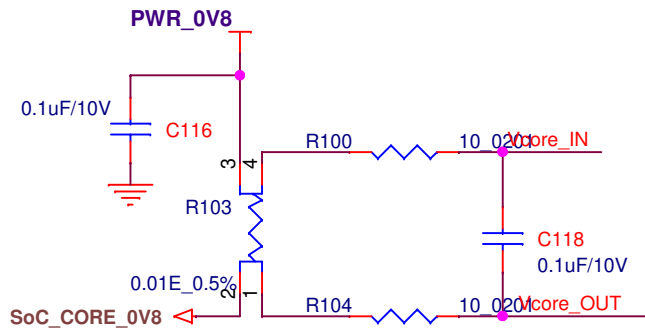


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